ABSTRACT OF THE DISCLOSURE

# INTEGRATED CIRCUIT WITH STOP LAYER AND ASSOCIATED FABRICATION PROCESS

A method for fabricating an integrated circuit. According to the method, a second dielectric layer is formed above a first dielectric layer, and holes and/or trenches are etched in the first and second dielectric layers. The holes and/or trenches are filled with metal in order to form electrical connection elements, and at least a third dielectric layer is formed. Holes and/or trenches are selectively etched in the third dielectric layer and the second dielectric layer with respect to the first dielectric layer and the elements, in order to control the depth of the etch. Additionally, there is provided an integrated circuit of the type having metallization levels separated by dielectric layers and metallized vias connecting lines of different metallization levels. The integrated circuit includes first and second metallization levels, first and second superposed dielectric layers located above the first metallization level, and a third dielectric layer located above the first and second dielectric layers. Further, at least one electrical connection element is provided in the third dielectric layer and passes through the second dielectric layer until it comes into contact with the first dielectric layer.



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